EXPRESS MAIL LABEL NO:
EL707908103US

METHOD OF REDUCING DISTURBS IN NON-VOLATILE MEMORIES

ABSTRACT OF THE DISCLOSURE

In a non-volatile memory, the displacement current generated in non-selected word lines that results when the voltage levels on an array's bit lines are changed can result in disturbs. Techniques for reducing these currents are presented. In a first aspect, the number of cells being simultaneously programmed on a word line is reduced. In a non-volatile memory where an array of memory cells is composed of a number of units, and the units are combined into planes that share common word lines, the simultaneous programming of units within the same plane is avoided. Multiple units may be programmed in parallel, but these are arranged to be in separate planes. This is done by selecting the number of units to be programmed in parallel and their order such that all the units programmed together are from distinct planes, by comparing the units to be programmed to see if any are from the same plane, or a combination of these. In a second, complementary aspect, the rate at which the voltage levels on the bit lines are changed is adjustable. By monitoring the frequency of disturbs, or based upon the device's application, the rate at which the bit line drivers change the bit line voltage can be adjusted. This can be implemented by setting the rate externally, or by the controller based upon device performance and the amount of data error being generated.

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